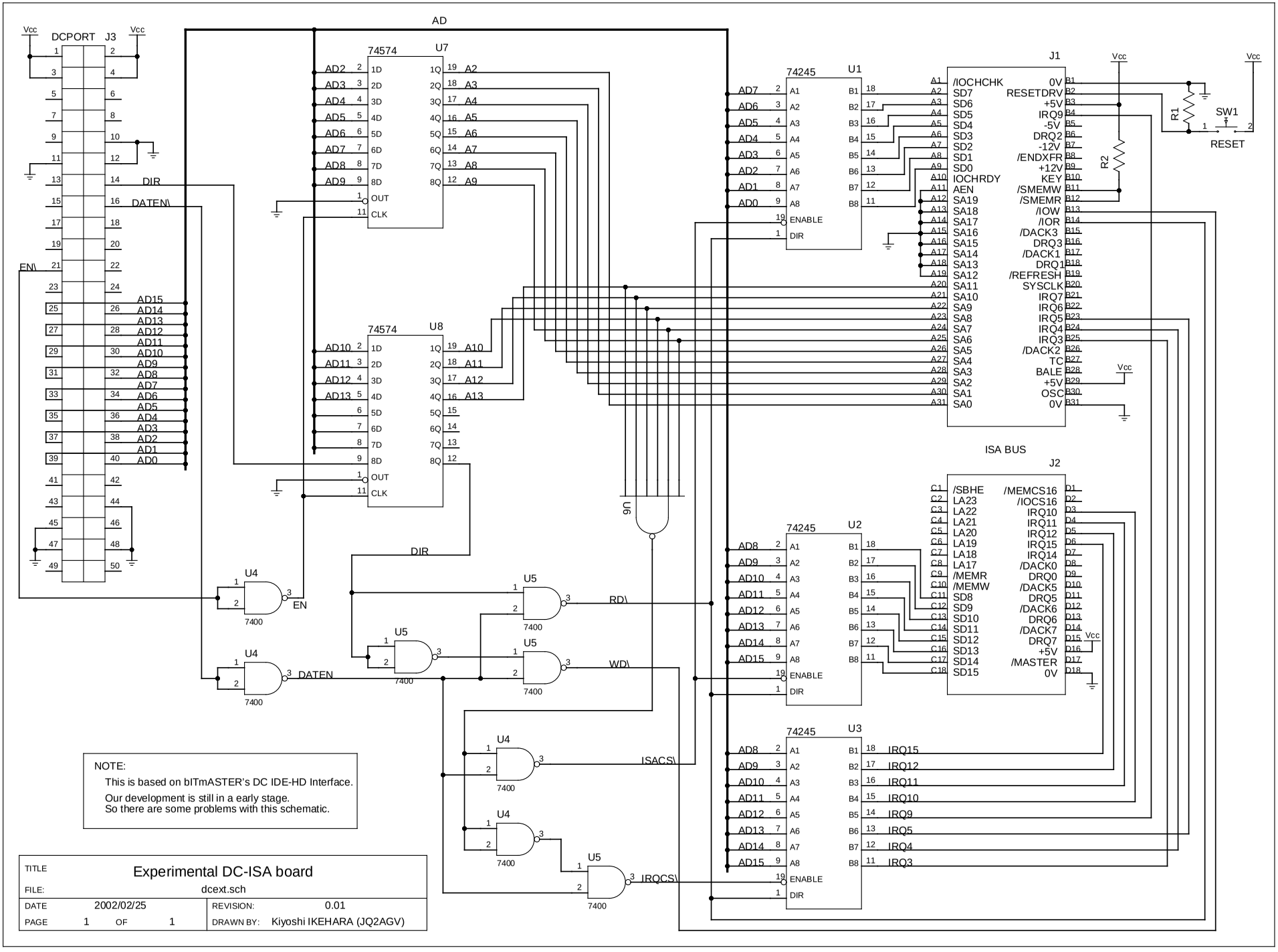
DCPORT J3
Vcc
DIR
DATEN\
EN\
AD15
AD14
AD13
AD12
AD11
AD10
AD9
AD8
AD7
AD6
AD5
AD4
AD3
AD2
AD1
AD0
AD
74574 U7
74574 U8
OUT
CLK
74245 U1
74245 U2
74245 U3
ENABLE
DIR
J1
/IOCHCHK
SD7
SD6
SD5
SD4
SD3
SD2
SD1
SD0
IOCHRDY
AEN
SA19
SA18
SA17
SA16
SA15
SA14
SA13
SA12
SA11
SA10
SA9
SA8
SA7
SA6
SA5
SA4
SA3
SA2
SA1
SA0
0V
RESETDRV
+5V
IRQ9
-5V
DRQ2
-12V
/ENDXFR
+12V
KEY
/SMEMW
/SMEMR
/IOW
/IOR
/DACK3
DRQ3
/DACK1
DRQ1
/REFRESH
SYSCLK
IRQ7
IRQ6
IRQ5
IRQ4
IRQ3
/DACK2
TC
BALE
+5V
OSC
0V
R1
R2
SW1
RESET
ISA BUS
J2
/SBHE
LA23
LA22
LA21
LA20
LA19
LA18
LA17
/MEMR
/MEMW
SD8
SD9
SD10
SD11
SD12
SD13
SD14
SD15
/MEMCS16
/IOCS16
IRQ10
IRQ11
IRQ12
IRQ15
IRQ14
/DACK0
DRQ0
/DACK5
DRQ5
/DACK6
DRQ6
/DACK7
DRQ7
+5V
/MASTER
0V
U4
U5
U6
7400
EN
DATEN
RD\
WD\
ISACS\
IRQCS\
IRQ15
IRQ12
IRQ11
IRQ10
IRQ9
IRQ5
IRQ4
IRQ3
NOTE:
This is based on bITmASTER's DC IDE-HD Interface.
Our development is still in a early stage.
So there are some problems with this schematic.
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Experimental DC-ISA board
FILE:
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DRAWN BY:
Kiyoshi IKEHARA (JQ2AGV)